

# II

## Designing Converters

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### Chapter 2

In Chapter 1, “Understanding Converters,” there is included a hasty survey of the more-popular converter design approaches. The intention of this chapter is to provide more-detailed and practical information on the design and construction of D/A and A/D converters for the benefit of both users and designers.

While one could recall the approaches described in the earlier chapter, but cover them in much greater depth, it is manifestly evident that to do justice to a number of the most popular designs would require more space than is available here. We have therefore decided to focus on one approach and attempt to treat it thoroughly.

The design approach chosen for D/A conversion uses quad current switches of the AD550 family and a monolithic thin-film resistor network of the AD850 type. The A/D conversion example uses this D/A converter in a successive-approximation device.

This practical example will serve the reader’s purposes well, and for a number of reasons. First, it represents an approach actually used for the construction of converters in production quantities, to be sold at competitive prices, with resolutions ranging from 8 to 16 bits. In addition, it has speed adequate for most purposes; the appropriate components are accessible to the designer at reasonable cost from at least one source (Analog Devices); and, having moderate complexity, it is an excellent starting point for understanding other designs of both greater and lesser complexity.

With this view of the inner workings of products engineered for OEM users (probably the first time a module manufacturer has

ever “told all”), users of converters may gain better insight into the devices they are using, and design engineers may gain some ideas or principles that will help them in their future designs.

## CONVERTER DESIGN

Many writers on this subject claim that a high-precision D/A converter is the most-difficult-to-design section of any device using it, including an A/D converter. This is only partially true; the added design elements, circuiting, and physical layout involved in using a D/A converter in an A/D converter should not be slighted. The increase of difficulty in building A/D converters of high speed and accuracy, even with a well-designed basic D/A-converter building block, can be massive.

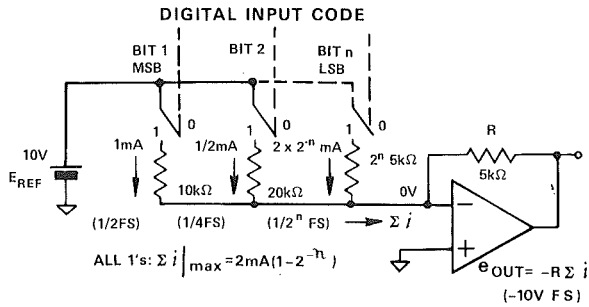
The difficulties of designing D/A converters increase rapidly with the useful resolution sought in the design. 8-bit D/A converters are relatively easy to design and manufacture, since the allowable uncertainty is of the order of 0.2%. Ten-bit converters are much more difficult to design, since the resolution sought is 0.05%. By the time one reaches 12 bits of resolution (0.0125%), the design and manufacturing problems become acute. And 16-bit converters should be left entirely alone by the do-it-yourselfer.

In most cases where the make-or-buy decision involves large numbers of units, it may be comforting to follow the example of the mass-transportation officials who suggest: “. . . leave the driving to us,” for reliable, economical, and carefree arrival at one’s destination.

## REVIEW OF D/A TECHNIQUES

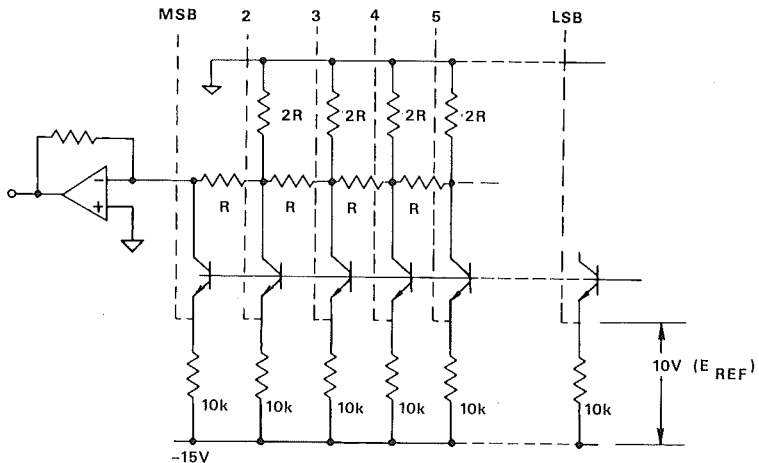
Figure 1 reproduces the current-weighting D/A converter depicted in Figure 14 of “Understanding Converters.” This is perhaps the simplest approach to performing a digital-to-voltage conversion. A set of binary-weighted currents flows through a  $5k\Omega$  feedback resistor, producing an analog output voltage proportional to the sum of those currents that are turned on.

While this approach looks simple, the problems of manufacturing a converter of this type are large. The two most difficult problems are the switching speed and resistor T.C. matching. For a 12-bit con-



*Figure 1. Elementary D/A Converter Circuit*

verter using a 10k $\Omega$  resistor for the most significant bit (MSB), the least-significant-bit resistor would be 40.96M $\Omega$ . This range of resistance cannot be obtained from a consistent film material, so that resistance temperature coefficients cannot even be approximately matched. Furthermore, the switching speed of a current switch depends upon the current available to charge the stray capacitances. Since the LSB is 0.5 $\mu$ A, if the stray capacitance is 10pF, then the settling time for 1LSB is 200 $\mu$ s. Obviously, if all currents could be of the order of 1mA, the conversion time for all bits will be uniformly shortened.

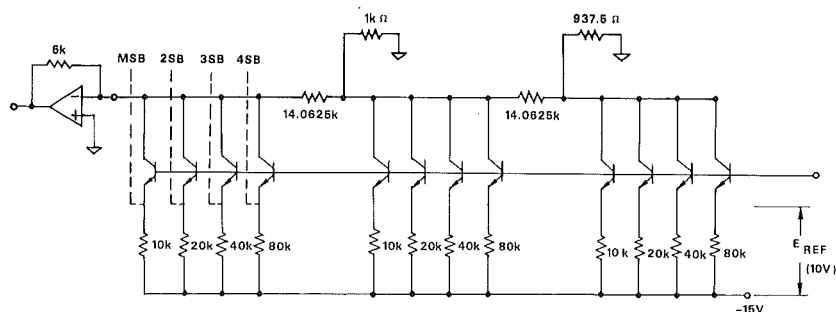


*Figure 2. D/A Converter Using Equal Current Sources and R-2R Ladder Attenuator*

Figure 2 shows a way in which this is commonly accomplished. Basically, the NPN current sources are all made equal to 1mA.

The individual currents from the collectors of the current source transistors are subjected to binary weighting via the R-2R network. D/A converters of this type yield extremely high speed conversions (e.g., the MDA-10F settles in 50ns). Other advantages of this circuit are evident: the resistance range is very reasonable and the selection of transistors for matched  $V_{BE}$  is simplified. However, a disadvantage of this circuit is that it requires *two* accurately-trimmed low-T.C. resistance networks.

A third technique (Figure 3) combines good features of both techniques. Commonly known as the quad current-source approach (see Figure 20 in the preceding chapter), the technique relies on binary-weighted current sources, in groups of four, with currents ranging from 1mA (MSB) to 1/8mA. Three such quads provide 12 bits of resolution. The currents from the third quad are resistively attenuated by 16:1 before summing with the currents in the second quad, and this sum is again attenuated by 16:1 before summing with the first quad's currents. Much of the circuitry, being repetitive, is highly amenable to monolithic integration, as exemplified by Analog Devices' AD550/AD850 monolithic  $\mu$ DAC conversion components.



*Figure 3. D/A Converter Using Binary-Weighted Quad Current Sources*

## THE IMPORTANCE OF LOGIC BUFFERING

The manner in which the switching signals from logic circuits are buffered from the analog circuitry of D/A converters, though of great importance, is not commonly well-understood. There are many ways (some good, some not so good), to turn electronic switches on and off. The simplest is the single diode approach shown in Figure 4 (see also Figure 19 in the preceding chapter).

Here the common base line of the current sources is biased at a midrange value of the TTL threshold (1.4V). When the data inputs are low ("0"), the diodes are forward-biased and draw the bit current away from the PNP current source. This, in effect, back-biases the PNP emitter-base junction, turning the transistor off. When the logic input goes high ("1" – greater than 2.0V), the diode is back-biased and the transistor current source is turned on.

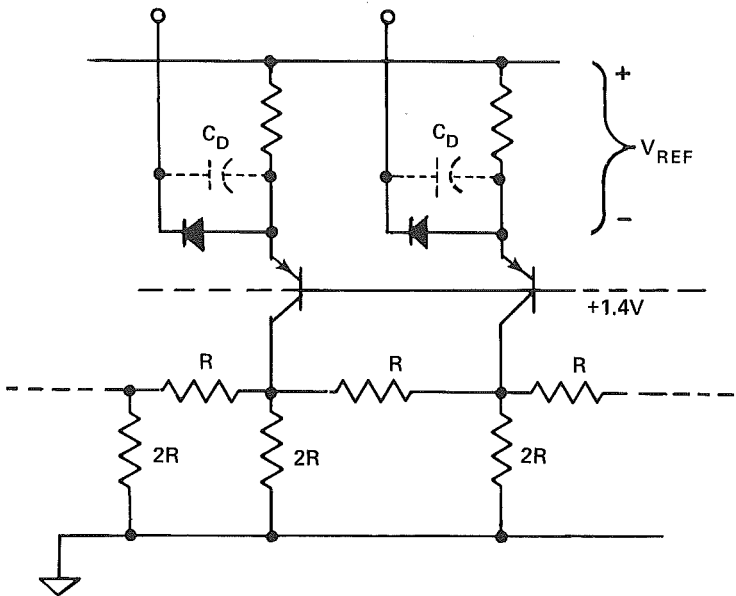
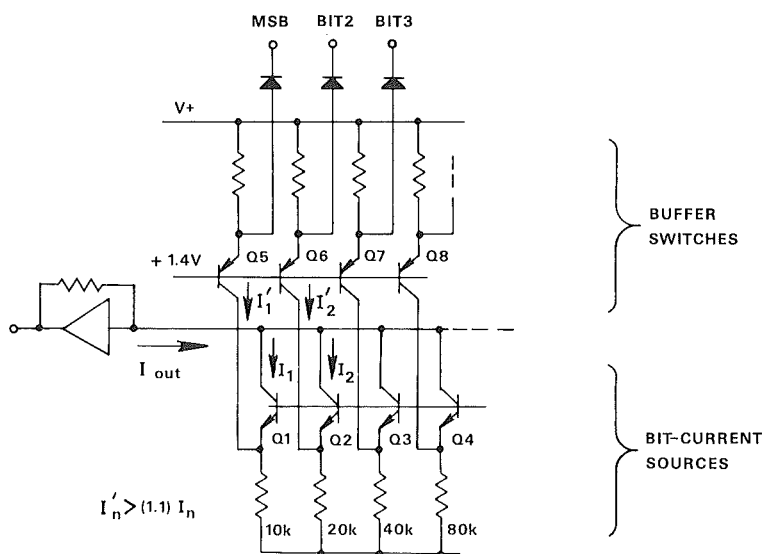


Figure 4. Diode Switching in D/A Converter

Two major error sources are characteristic of this simple approach. The first is leakage current in the diode. 10nA may sound negligible at room temperature, but at 70°C this figure is in the neighborhood of 1μA, an appreciable error. Similarly, when the switch is in the high state, the diode is back-biased; logic transients on the data input side, though not of sufficient magnitude to affect the switch state, are coupled through the diode capacitance, to the emitter of the current source, thereby producing transient errors in the weighted current.

Figure 5 shows a much-improved way to electronically switch current sources on and off. This buffered scheme involves essen-

tially two D/A converters. The first, using Q1–Q4, performs the actual high-accuracy conversion. The second D/A, composed of Q5–Q8, accepts the digital inputs and applies back-bias to the emitters of the appropriate switching transistors, Q1–Q4, as required by the input code (which must be complementary to the input code required by the circuit in Figure 4). For example, when the input logic at Q5 is high, the diode is reverse-biased and Q5 conducts. Its positive collector current biases the emitter of Q1 high and effectively diverts the flow of  $I_1$ . When the logic input is low, the diode shuts off Q5's collector current, which allows  $I_1$  to flow normally in the collector circuit of Q1. The buffered scheme solves both problems of the single-diode approach.



*Figure 5. Buffered Switches in D/A Converter*

Often overlooked in the buffer design is how much swing must be provided at the emitter of Q1 to toggle the switch fully from *on* to *off*. The following exercise may be revealing:

$$\Delta V_{BE} = \frac{kT}{q} \ln \frac{I_{ON}}{I_{OFF}}$$

For 12-bit resolution, with 1/10LSB uncertainty,

$$\frac{I_{ON}}{I_{OFF}} > 10 \times 2^n \cong 40,000$$

Since  $\ln(40,000) \cong 10.5$ , at  $70^\circ\text{C}$  ( $343^\circ\text{K}$ )

$$\Delta V_{BE} = 29\text{mV} \times 10.5 = 300\text{mV}$$

and, at  $125^\circ\text{C}$ ,

$$\Delta V_{BE} = 33\text{mV} \times 10.5 = 350\text{mV}$$

If one considers that the standard TTL input logic thresholds are 0.8V for "0" and 2.0V for "1", and that diode drops, while conducting  $I_{ON}$ , may approach 0.7V, it is evident that the base line must be held within a narrow range of voltage, especially at higher temperatures.

## MONOLITHIC COMPONENTS

The basic monolithic conversion components to be discussed in connection with the circuitry encountered in the remainder of this chapter are the AD550 monolithic quad switches and the AD850 monolithic thin-film resistor network.

The key factor establishing the accuracy of the quad switches is the binary weighting of the current-source transistors, Q1–Q4 in Figure 6. It is well known that two matched transistors, operating at current densities that cause the  $V_{BE}$  drops of the transistors to be equal, will exhibit theoretically perfect tracking with temperature.

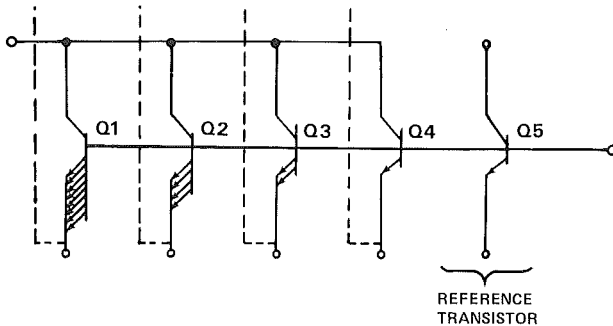
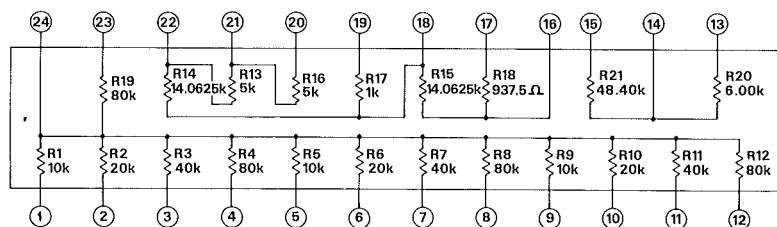


Figure 6. Binary-Weighted Current Source Transistors

If two perfectly-matched paralleled transistors together draw twice the total emitter current of a third matched transistor, their  $V_{BE}$ 's will nevertheless be equal.

The current switches Q1–Q4, though conducting currents in the ratio 1:2:4:8, have similarly-weighted emitter areas, hence equal current densities, and will therefore exhibit equal  $V_{BE}$ 's. If the  $V_{BE}$  drops of the current sources are equal, then errors in current due to variations of  $V_{BE}$  in series with the measuring resistors track perfectly for all four switches.

The finite  $\beta$  of the current-source transistors represents another source of conversion error, since the base current,  $I_E/(1 + \beta)$  subtracts an increment from the emitter current. Monolithic construction leads to initial  $\beta$ -matches within  $\pm 5\%$ . When used with the reference transistor, Q5, the effects of both  $V_{BE}$  and  $\beta$  variation with temperature can be fully compensated, resulting in extremely low temperature coefficients for the conversion.



R 1	10k REF	0.1% ABS	R 8	80k	0.8%	R15	14.0625k	1.0%*
R 2	20k	0.015%	R 9	10k	1.0%	R16	5k	0.1%
R 3	40k	0.03%	R10	20k	1.0%	R17	1k REF	0.1% ABS
R 4	80k	0.05%	R11	40k	1.0%	R18	937.5Ω	1.0%*
R 5	10k	0.1%	R12	80k	1.0%	R19	80k	0.1%
R 6	20k	0.2%	R13	5k	0.1%	R20	6.00k	0.1%
R 7	40k	0.4%	R14	14.0625k	0.1%*	R21	48.40k	0.1%

**NOTES:**

All resistors ratio to R1 except R14, R15, R18 which ratio to R17. Tolerances shown are for 12-bit accuracy and degrade by factor of four maximum for 10-bit accuracy.

Total positive or negative "contribution to error" is less than 0.012%  
BCD network, AD851, is:  $R_{13} = R_{16} = 4k\Omega$ ;  $R_{14} = 8.1325k\Omega$ ;  
 $R_{15} = 8.4375k\Omega$ .

*Figure 7. Typical Monolithic Thin-Film Resistor Network (AD850)*



The companion AD850 thin-film resistor network is shown schematically in Figure 7. Included in this network are:

- Bit-weighting resistors (R1 – R12)
- Reference compensation resistor (R19)
- Interquad divider resistors (R13, R14, R15, R17, and R18)
- Gain resistors (feedback resistor in D/A's, input resistor in A/D's) (R13 and R16)
- Reference input resistors (R21 and R20)

When used for all its indicated circuit functions, this resistor network has the interesting property that, as long as the resistors track one another as temperature changes, the output voltage error due to absolute resistance changes for any given code combination will be nil. The reason is that absolute resistance changes of *all* resistors in the network make little difference – the tracking *between* resistors is the only item of importance. For the AD850, temperature coefficient of tracking error is  $\pm 1 \text{ ppm}/^\circ\text{C}$ .

### COMPONENT TOLERANCE

Save for the reference and output amplifier, the errors produced by the analog components used to build a D/A converter can be mainly attributed to errors caused by the bit switches and resistance tolerances. The  $V_{BE}$  and  $\beta$  mismatch errors in the quad current switches have already been briefly touched upon. Naturally, the tracking of these parameters with temperature influences errors measured when temperature changes.

The Analog Devices AD550 is classified into numerous parametric categories. On the data sheet, 30 of these categories are shown. The three main subdivisions relate to the relative contribution to error by each bit. The “J” grade ( $\pm 1\%$ ) is used in the least-significant-quad position. The “K” grade ( $\pm 0.1\%$ ) is used in the middle quad of 10- or 12-bit converters. The “L” grade ( $\pm 0.01\%$ ) is used in the most significant quad position. The other 10 subdivisions result from sorting these units by  $V_{BE}$  at rated current. The  $V_{BE}$  range from 600mV to 700mV is subdivided into the 10mV categories denoted by the integers 0 to 9 (i.e., 600–609, 610–619, etc.)

Interquad  $V_{BE}$  matching is required to minimize errors between bits in the first quad and bits in the second quad. If the  $V_{BE}$  difference between Quad 1 and Quad 2 were 100mV, then the apparent error in bit 5 relative to full scale would be 0.03%. When the three AD550's used in a 12-bit converter are assembled, the  $V_{BE}$  groupings of at least the L and K grades must match.

Internally, at ADI, the product breakdown is even more detailed than is indicated on the AD550 data sheet. The AD550L, which fortunately has quite respectable yields, is itself graded and further subdivided into higher-accuracy groups designated as follows:

Switch Contribution to Error  
(Relative to MSB)

Grade Designation	Switch Matching Error
LA	0.01%
LB	0.007%
LC	0.005%
M	0.002%

The errors listed for each grade are maximum, as measured in an actual conversion circuit. Thus, they are a composite of  $V_{BE}$  and  $\beta$  tracking errors, and take advantage of compensation, where it occurs. As indicated, these subdivisions are mainly for internal manufacturing purposes, but the user of AD550's may be comforted to know that when he orders an "L" grade unit, he nearly always gets, in actuality, an LC. The M-grade unit is used for the most-significant quad in the DAC-16QM (and ADC-16QM).

The resistor specifications listed in the table (Figure 7) are often misinterpreted. It is imperative that a D/A-circuit designer understand the meaning of the tolerance specifications, and their effect on a given resistor's contribution to the total error. The most-significant-bit resistor, R1, is used as the reference resistor for ratio-matching purposes; all the other resistors are referred to it. The second-bit resistor, R2, is shown as having a ratio tolerance of 0.015%. Some persons automatically interpret this as meaning that the second-bit resistor could contribute an error of 0.015% *relative to full scale*. This interpretation is wrong. Since the MSB (R1)

has a weight of  $\frac{1}{2}$ F.S., the second-bit contribution to error has a weight of  $\frac{1}{4}$ F.S. This means that a ratio tolerance of 0.015% for  $R_2/R_1$  will cause bit 2 to have a contribution to full-scale error of  $\frac{1}{8}$  LSB of 12 bits (0.00375%).

Applying a tolerance analysis to the specifications, one might be led to expect that a 12-bit set of AD550's and an AD850, when assembled (with the best of care) will always yield a 12-bit-linear D/A converter, with no bit-trimming necessary. The overall error actually depends upon a statistical distribution of the errors of both sets of components. In the very worst case, it is possible for some code combinations to be outside the 12-bit linearity expected. For this reason, we recommend certain final-trimming procedures, which will be described later. Besides being occasionally necessary, they lead to improved temperature-margins and a sense of confidence that each assembled unit is well within specifications.

## THE INTER-QUAD DIVIDER

The inter-quad division network of the AD850 functions quite simply. The basic idea is depicted in Figure 8a, where a current source delivers its current to the node joining a  $15k\Omega$  resistor and a  $1k\Omega$  resistor. Since the  $15k\Omega$  unit is terminated in virtual ground (the amplifier summing junction), the voltage across both resistors will be equal. Hence,  $\frac{15}{16}$  of the original current ( $I$ ) goes off to signal ground via the  $1k\Omega$  resistor, while the remaining

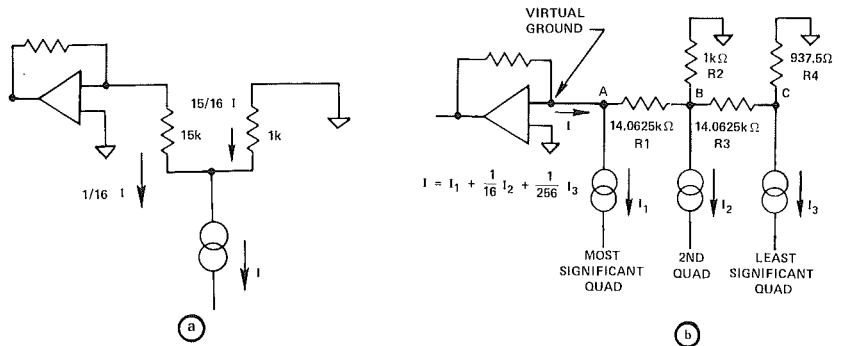


Figure 8a. Current Attenuation to 1/16

Figure 8b. Current Attenuation of Three Sources to 1, 1/16, 1/256

$1/16 I$  is added at the summing point via the  $15k\Omega$  resistor. The problem is just a little more complicated when the multiple-current-source situation depicted in Figure 8b exists.

In Figure 8b is a simplified diagram of the AD550 outputs and the interquad weighting resistors of the AD850. The 3 current sources  $I_1$ ,  $I_2$ ,  $I_3$ , represent the common collector lines of the three quads. The current from the most-significant quad (MSQ) flows directly into the summing node of the op amp (virtual ground). The second quad's current is split 16:1 by the following means: As the current enters node "B",  $15/16$ ths of  $I_2$  goes to signal ground through the parallel combination of  $R_2$  with  $(R_3 + R_4)$ . The remaining  $1/16$  goes off through  $R_1$  to the summing node "A". Note that the parallel combination of  $R_2$  and  $R_3 + R_4$  is  $937.5$  ohms. Thus, the inter-quad current split effected at node "B" is precisely 16:1.

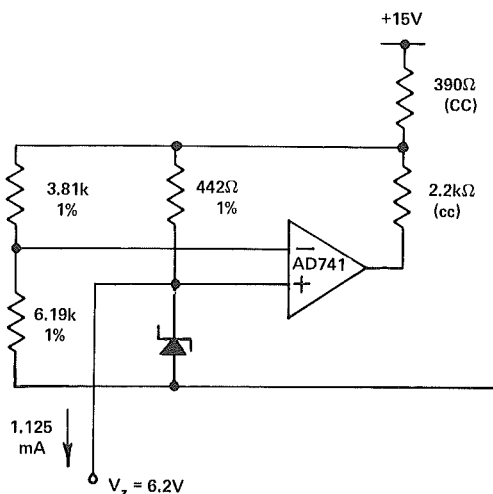
The inter-quad current division at node "C" is a little more difficult to understand. It is easiest to analyze the two interquad dividers as a single network and solve for a 256:1 attenuation of  $I_3$  as it reaches node "A". By a straightforward analysis, one can learn that the current entering node "B" from node "C" is  $1/17 I_3$ . At this point, it is further split, in the ratio 15.0625:1, by  $R_1$  and  $R_2$ . The product of 15.0625 and 17 is, as desired, 256.

One should note that, in the practical situation, the current sources depicted at Figure 8 are the collectors of common-base NPN transistors. The designer must be aware of the fact that when all bits are turned on, a voltage drop appears at nodes "B" and "C" of the order of  $-1.8V$ . For this reason, the common base line of the current sources should be operated below  $-2.0V$ , in order to keep the transistors well within their linear region. Also, it should be noted that the output resistance of the collectors in the most-significant quad can be as low as  $30M\Omega$  without significantly affecting divider accuracy.

## REFERENCE LOOP

The overall gain and accuracy of a D/A converter depend on that of a stable current reference. The AD550/AD850 system is designed to use the common  $6.2V$  "zero-T.C." zener reference diodes.

Figure 9 shows one such diode, the 1N829A, used in a circuit that provides it with an essentially constant-current drive. Low-T.C. zeners require 7.5mA of constant bias current to maintain minimum temperature coefficient. Furthermore, variations of the current with temperature or supply voltage will alter the zener voltage, due to the drop across the diode's  $R_{on}$  (about  $10\Omega$ ). The circuit of Figure 9 provides excellent power-supply rejection and a sufficiently accurate 7.5mA bias current, plus the 1.125mA taken by the input current of the converter's reference amplifier and the bipolar offset, used in the recommended AD550/AD850 combination. The  $2.2k\Omega$  resistor at the output of the AD741 op amp helps maintain the amplifier in its linear region by reducing its output load, which it shares with the +15V supply. It also avoids latchup.



*Figure 9. Constant-Current Excitation of Precision Reference Zener Diode*

The basic reference loop for the D/A converter is shown in Figure 10. The reference transistor of the most significant quad (see Figure 6) is used to monitor changes in the  $V_{BE}$  and current gain of all the bit switches (since it is identical to them and operating under virtually identical conditions). The zener voltage, developed as in Figure 9, is connected to pin 14 of the AD850 ladder network.

A trim resistor, placed in series with the  $48.4k\Omega$  (R21) reference-current resistor, allows the current supplied, via the op amp's

summing junction, to the collector of the MSQ reference transistor, to be adjusted to just  $1/8\text{mA}$ . Since the reference transistor has the same geometry as each elementary bit-transistor, the resistors are precisely weighted, and all transistors share a common voltage-reference supply, then when the reference loop has adjusted the base voltages such that  $0.125\text{mA}$  flows in the collector of the reference transistor, the properly-weighted currents will automatically flow through the collector circuits of all turned-on bit-switches.

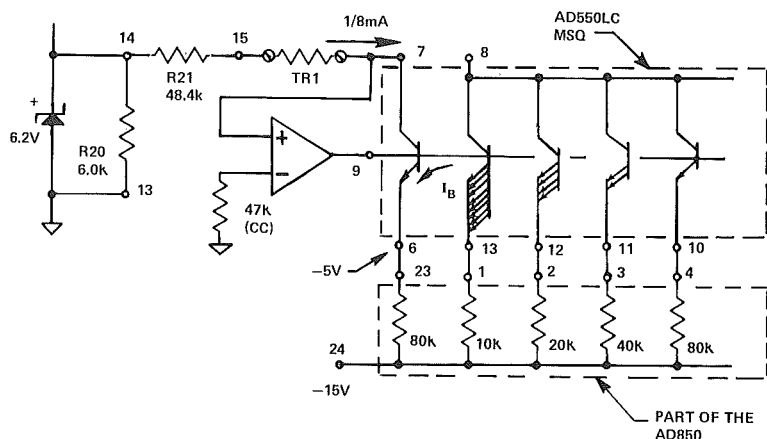


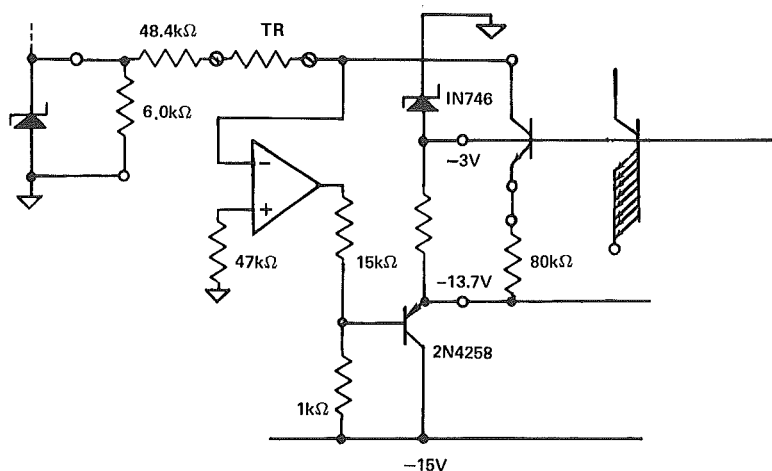
Figure 10. Reference Circuit Using Non-inverting Amplifier Input

As the  $V_{BE}$ 's and current gains of the transistors change with temperature, the reference loop will adjust the base voltages to track and maintain  $1/8\text{mA}$  at all times into the reference transistor's collector, and correspondingly proportional currents through all the other collectors. Adjusting the value of the trim resistor  $TR_1$  will adjust the absolute value of the reference current and hence all of the individual bit weights in proportion. The  $48.4\text{k}\Omega$  reference current resistor  $R_{21}$  is designed to produce  $1/8\text{mA}$  with a minimum zener voltage of  $6.05\text{V}$ , with  $TR_1 = 0$ .

The configuration of Figure 10 is simple and can be easily described; however, it is prone to latch up under certain conditions because it uses the op amp's positive input. For certain sequences of power-supply turnon, it is possible for the amplifier output to become positive with respect to ground, thereby forward-biasing the base-collector junction of the reference transistor and latching

the amplifier in its positive feedback mode. The inverting configuration of Figure 11 avoids this problem by adjusting the common side of the supply, instead of the base line, to close the loop.

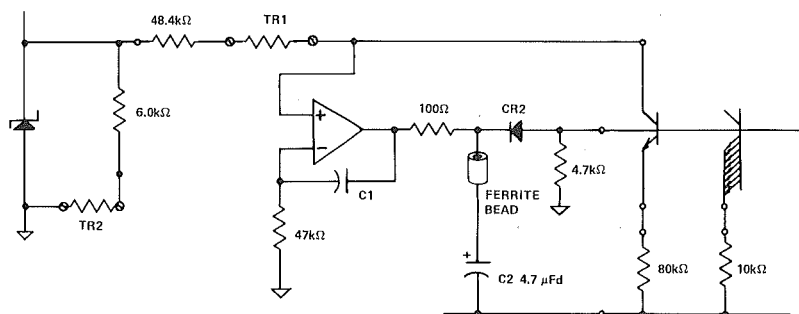
Here the common base line is biased by the 1N746 at  $-3\text{V}$ . The inverting op amp drives the resistors' common rail via a buffer and level shift circuit. Another advantage of this circuit is improved immunity to noise in the  $-15\text{V}$  supply. Unfortunately, it has the disadvantage that it is difficult to prevent the circuit from bottoming on the  $-15\text{V}$  rail, since the base of the PNP buffer is within  $0.6\text{V}$  of the  $-15\text{V}$  line.



**Figure 11. Reference Circuit Using Inverting Input**

In Figure 12, the basic non-inverting configuration of Figure 10 is revised to include an anti-latchup circuit — CR2 and the 4.7k $\Omega$  resistor. It also includes frequency-response shaping to prevent transient voltages from upsetting the reference loop, as follows: In junction-isolated IC's, such as the AD550, capacitive coupling from the collector of one NPN transistor to the collector of another NPN transistor exists via the depletion capacitance of the substrate. When the input bit combination changes, the DAC's output amplifier will usually be driven in a slewing condition, resulting in a fast rising voltage edge on the common collector line of the AD550. This fast-moving edge is coupled to the collector of the reference transistor on the same chip. Since the collector of the

reference transistor looks at a high impedance ( $48.4\text{k}\Omega$ ), the coupled transient is applied to the noninverting terminal in the circuit of Figure 10. This, in turn, can upset the reference loop for a period of microseconds.



*Figure 12. Reference Circuit With Frequency Shaping and Anti-Latchup Circuit*

In the configuration of Figure 12, we can see a means by which this behavior can be controlled. The voltage from the common base rail of the AD550 to  $-15\text{V}$  is kept from changing instantaneously by a  $4.7\mu\text{F}$  capacitor. However, since a  $4.7\mu\text{F}$  capacitance can by itself cause the reference amplifier to oscillate, a  $100\Omega$  isolation resistor provides a predictable time constant. C1, together with the  $4.7\text{k}\Omega$  common-mode bias-compensation resistor, rolls off the response of the amplifier on a  $6\text{dB/octave}$  slope, which intersects unity open-loop gain at the breakpoint of the  $100\Omega \times 4.7\mu\text{F}$  combination. CR2 and the  $4.7\text{k}\Omega$  resistor prevent the latchup mode mentioned earlier. The ferrite bead is added to prevent the common-base bit-switches (with  $f_t$ 's of approximately  $500\text{MHz}$ ) from oscillating in the  $100\text{--}200\text{MHz}$  region.

The  $6.0\text{k}\Omega$  resistor on the AD850 (R20) is shown connected to signal ground in Figures 10, 11, and 12. R20 provides  $1\text{mA}$  offset current in bipolar offset-binary D/A converters, when it is connected to the output current terminal of the converter. This resistor should be grounded when the unipolar configuration is desired, so that the zener diode (Figure 9) runs at constant current. Ignoring this consideration — leaving R20 open — can result in a gain error of  $0.2\%$ . Of course, with an external reference, or with a



circuit in which the reference voltage is applied via a low impedance (e.g., the emitter of an inside-the-loop follower) it would not matter greatly whether or not R20 were terminated.

## TRIMMING HIGH-ACCURACY CONVERTERS

One should be always aware that, however easily we may talk of 12-bit accuracy, it still represents *total error* of the order of 0.01%, which many circumspect engineers still consider uncomfortably-close to the limits of the state-of-the-art. Second- and third-order tolerance buildups can become highly significant, as can inadvertent errors in interfacing a converter with its analog output circuit or a measurement circuit.

For 12-bit (and better) linearity, the designer of converters should always seek *the best-possible resolution*, and should make provisions for final trim of the highest-order bits in order to attain it. In addition, he must provide both coarse and fine trims of the overall "gain" (i.e., scale factor) of the converter, offset-bias-current trim for bipolar converters, and overall zero adjustment of the output amplifier.

Let us start with the bit-trimming procedures. The AD550 and AD850, in combination, are amenable to highly-accurate and stable trimming. Figure 13 is a fairly-complete schematic of the first

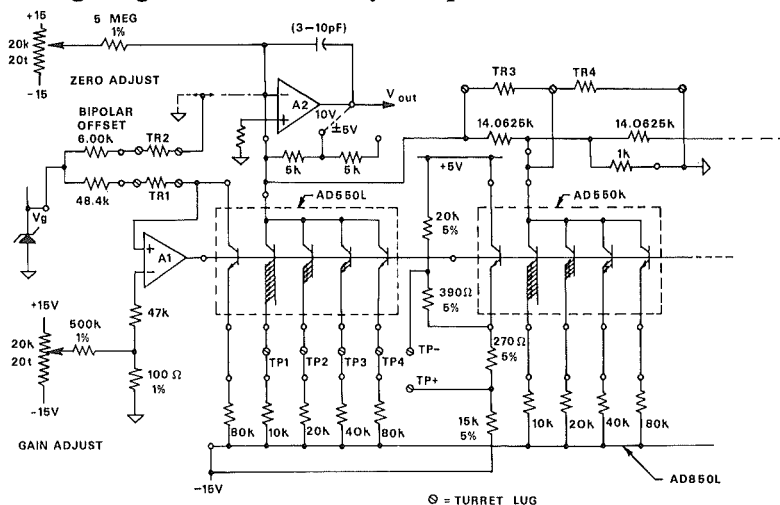


Figure 13. Connections for Trimming a D/A Converter for 12-Bit Accuracy

8 bits of a 12-bit D/A; it will illustrate the discussions to follow on trimming and adjustment.

For final trim of the first 4 bits, a number of nanoamperes of current must be added to or subtracted from the emitter current of each switch to bring it to its calibrated relative value. To do this, we use the conveniently-available reference transistor of the second quad (AD550K) to establish two small offset voltages, which will be centred about the emitter voltage of the bit-switches. In Figure 13, the AD550's reference transistor is biased by approximately 1/8mA; ordinary carbon composition resistors may be used. The voltage at TP+ is 200mV *below* the emitter voltages, while that at TP- is 200mV *above* the emitters. These arbitrary designations are for convenience in trimming.

If the bit being adjusted does not have sufficient weight (measured at the output, using instrumentation of adequate precision), a current  $\Delta I$  is added to that bit by connecting a resistor of appropriate value ( $R = 200\text{mV}/\Delta I$ , or conductance 2.5 micromho/LSB) from the emitter of the bit switch in question to TP+. Similarly, if the bit weight is too high, it can be decreased by connecting an appropriate resistance between the emitter and TP-. It should be noted that, as temperature varies, the  $V_{BE}$  of all the transistors will also vary. But the trim voltages will remain fairly constant and centred around the nominal emitter voltage of the AD550k's reference transistor.

To minimize the effects of slight mismatches between the first two quads, due to either  $V_{BE}$  or  $\beta$  differences, one should provide for slight trimming of the first interquad divider (i.e., the relative weight of the second quad). If, after trimming the first four bits, the fifth bit differs from  $\frac{1}{2}$  the fourth bit by a significant amount, the following procedure may be followed:

If bit 5 is too *low* in weight, install a trim in the TR3 position (usually of the order of megohms). If bit 5 exhibits *too much* weight, it can be attenuated with a trim in position TR4 (typically of the order of 100k $\Omega$  or more).

Normally, 1/8W carbon-composition resistors can be used in these positions, since only very small quantities of current are drawn

through them. The carbon-composition-resistor temperature coefficients are attenuated by both their overall weight relative to the resistors they parallel, and the bit weight, relative to full scale. This effect is negligible.

To trim the overall gain of a converter, trim-position TR1 is utilized. First center the gain-adjust pot (10 turns from one end). Install a decade-resistance box for TR1, and turn on the first four bits (00001 . . . 1 in complementary binary). With the  $5k\Omega$  resistor serving as the feedback resistor for the output amplifier, the proper output voltage should be 0.3750 (unipolar mode) for best adjustment of TR1. Replace the indicated decade resistance by the nearest standard precision-film-resistance value. (R20 of the AD850 should be grounded during this operation). Final gain trim can now be accomplished with the trim resistance installed in TR1. The resistance values shown in Figure 13 provide a mean adjustment of  $\pm 0.25\%$ .

To adjust zero in unipolar converters, turn off all bits (1 1 1 . . . 1 in complementary binary), and adjust "Zero Adjust" for 0.0000V out. In bipolar converters, to trim the bipolar offset ( $\pm 5V$  full-scale output range), center the 20-turn "zero-adjust" pot and connect the bipolar offset resistor to the output amplifier's summing point, as indicated in Figure 13. Using a decade box in TR2, and leaving all bit switches off, adjust the decade box for  $-5.0000V$  out. Install the nearest value of trim resistance to the reading of the decade box in the TR2 position. Final offset trim can now be performed with the MSB only on (0 1 1 1 . . . 1 in complementary offset binary) using the "zero-adjust" pot.

Further details on testing procedures and trimming of D/A and A/D converters can be found in chapter 3, "Testing Converters." An additional detail of the design of the circuit of Figure 13 is worth mentioning:

The feedback capacitance (3 to  $10pF$ ) around the output amplifier compensates for the capacitance of the common collector rail of the AD550L, the input capacitance of the output amplifier, and circuit strays. Circuit wiring capacitances should, of course, be minimized to keep the value of feedback capacitance low, since it tends to increase the output settling time. It is adjusted for

“optimum” response: minimum transients *and* settling time. Its omission may cause oscillations, or instability.

## TEMPERATURE VARIATION EFFECTS

Reiterating an earlier statement, if all resistors in the AD850 network track perfectly, then even if their absolute value changes, say at a rate of  $50\text{ppm}/^{\circ}\text{C}$ , the output voltage will remain constant (assuming constant  $V_Z$ ). This can be shown by the following example: If the reference-current resistor ( $R_{21}$ ,  $48.4\text{k}\Omega$ ) increases by 2%, the reference current would be decreased by 2%. However, the feedback resistor around the output amplifier is also increased by 2%, increasing the gain by 2% to compensate, with no net error. Since the bipolar offset resistor,  $R_{20}$ , also increases in proportion, there is no net error in bipolar applications. Variation of the current-weighting resistors is compensated by similar variation of the resistance in series with the emitter of the reference transistor. And finally, the interquad attenuation resistors track one another and maintain constant attenuation of the outputs from the less-significant quads.

This example describes the ideal situation. In practice, the resistance values will track ratiometrically to only about  $1\text{ppm}/^{\circ}\text{C}$ . Further, the discrete metal-film resistors used for  $TR_1$  and  $TR_2$  will undoubtedly have temperature coefficients that differ from those of the ladder resistors. Since their effect on total resistance is incremental, the effect of their T.C. on circuit performance is reduced. However, one should always perform a calculation to be sure that they can be safely neglected. Here is an example:

The absolute TCR of the AD850 is within  $\pm 25\text{ppm}/^{\circ}\text{C}$ . Assume that  $TR_1$  and  $TR_2$  have an absolute TCR range of  $\pm 50\text{ppm}/^{\circ}\text{C}$ . The effect of these mixed TCR's is dependent upon the absolute value of  $V_Z$ . The greater  $V_Z$  is, the larger the value of  $TR_1$  (and  $TR_2$ ). For  $V_Z = 6.5\text{V}$ , at the high end of a +5% tolerance range, the worst case of TCR mismatch will be approximately  $5\text{ppm}/^{\circ}\text{C}$  for a  $50\text{ppm}/^{\circ}\text{C}$  TCR of  $TR_1$ . If the TCR of  $TR_1$  is reduced to  $\pm 10\text{ppm}/^{\circ}\text{C}$ , this drift mismatch is reduced to  $2.5\text{ppm}/^{\circ}\text{C}$ . If the zener voltage is at its nominal value,  $6.2\text{V}$ , and  $TR_1$  is  $\pm 10\text{ppm}/^{\circ}\text{C}$ , then gain drift is reduced to approximately  $1\text{ppm}/^{\circ}\text{C}$ . Suffice it to

say that the closer  $V_Z$  is to the low end of its allowable tolerance range (6.05V), and the lower the TCR of the trim resistors is kept, the lower the effect of temperature on gain T.C. Then, scale factor (or gain) drift becomes almost entirely dependent on the Zener diode's voltage T.C.

Another contributor to gain drift is the offset drift, with temperature, of the reference amplifier, A1. Both offset voltage and bias current drifts must be considered. As an example, suppose that the total effect amounts to  $15\mu\text{V}/^\circ\text{C}$ . This will contribute roughly  $2.5\text{ppm}/^\circ\text{C}$  to gain drift ( $15 \times 10^{-6}/6.2 = 2.5\text{ppm}$ ). Gain drift error can also result from a reduction in open-loop gain of the output amplifier. For instance, a gain change, in A2, from 20,000 to 10,000, can result in an error contribution of 0.005%. It is therefore very desirable for A2's open-loop gain to be greater than 40,000 at room temperature.

## CURRENT VS VOLTAGE OUTPUT

A converter can be built to produce either an analog current output or an analog voltage output. The AD550/AD850 combination produces a basic current output, which is externally converted to a voltage using an additional output amplifier. However, since the op amp must slow down the response, some users prefer a current output for their application, or a passively-derived (small) voltage output.

Since the drift of the current output is not compensated by a tracking feedback resistor, the drift of current output from the D/A circuit in Figure 13, with the amplifier removed, is subject to the absolute TCR of the resistance ladder network, and can be as great as  $\pm 25\text{ppm}/^\circ\text{C}$ . The current output terminal of the D/A can be terminated in a resistive load to ground. However, one must observe the range over which this kind of loading is applicable. A total load resistance of  $1\text{k}\Omega$ , with  $2\text{mA}$  full-scale output current, will produce an output voltage of  $-2\text{V}$  full scale. Higher-value resistors will drive the common collector bus into saturation, producing excessive non-linearity.

Though it might appear at first glance that the interquad division ratios might be disturbed by using a resistive load instead of a virtual



ground, vigorous application of Norton's theorem will show that only the overall scale factor is affected. With a resistive load, the overall scale factor is determined by the external load, in parallel with the resistance looking back toward the interquad dividers (and — in the case of bipolar converters — the offset current resistor ( $R_{20}$ )).

If the output voltage developed across a passive load is to be amplified, attention must be paid to the common-mode and offset drift requirements of the output configuration and the choice of resistor ratio in the amplifier feedback circuit, especially if large amounts of gain are desired. The problem of gain temperature coefficient due to non-compensation of the absolute TCR by the unused built-in feedback resistor may be solved to a degree by using a discrete  $48k\Omega$  resistor, matching the TCR of the external load resistor, to set the reference current (and another matching resistor to replace  $R_{20}$  for bipolar applications). Though the loading effect of the interquad resistances will tend to worsen it, the gain-temperature coefficient will be greatly improved by good discrete-resistor tracking.

### ON ERROR BUDGETS

One can see, from the above discussion, that there are many sources of error. As desired resolution and linearity increase, and as first-order errors are decreased, the many sources that contribute 2nd and 3rd-order errors become more important. One way that some designers keep these sources in mind and try to account for their probable contributions is to use some form of error-budget analysis.

This consists of listing all the anticipated sources of error, with their expected worst-case and probable contributions, and using some form of linear or root-sum-of-the-squares summation to estimate the total error.

Error budget analysis, used as an intelligently-applied checklist, is at its most-useful in pinpointing those sources of error that must be minimized, either by circuit design, by trimming, by component selection, or by performing some cost tradeoff.

As a means of predicting total error, error budgets are no better

than the assumptions made, both about the individual error sources and about the way they will occur and combine when the circuits are assembled in production quantities. A too-conservative design for no-rejects, based on straight summation of worst-case errors, may result in greater overall cost of production than a less-conservative but more-clever design (utilizing some insight into how errors might combine), even though the less-costly design may (nay, *should*) produce (an acceptable number of) rejects in testing. (The cost of rejects can be reduced by recycling.) On the other hand, it is possible to defeat the best estimate of overall error by poor layout or component choice, or the best estimate of cost by requiring excessive tweaking or rejects.

### LAYOUT CONSIDERATIONS

Up to this point, we have dealt strictly with the electrical circuit design of digital-to-analog converters. We have discussed some of the finer points of error and drift compensation. Now let us turn our attention to those factors that do not show up in the schematic.

Sources of both static and dynamic errors must be considered when designing the layout of the converter. Static errors are most often caused by voltage drops in “ground loops” and result from carelessness in the layout process. To give an appreciation for how easily this problem can arise, consider a hypothetical example. Suppose an analog ground line has 50 milliohms of resistance between two points. Suppose the current variation through that piece of track is 0 to 10mA for various code combinations in the converter. The resulting change in ground potential is 0.5mV. If this ground happens to be in common with the output signal, this type of error can be disastrous in converter designs calling for 12-bit and better resolutions.

Furthermore, the selection of input/output sockets and pins is very important. It is not difficult to pick up 100m $\Omega$  of contact resistance in an improperly-chosen connector. Suffice it to say that all lines carrying analog output currents must be carefully located, and calculations should be performed to ensure that lead-resistance and ground-loop errors are minimal. Never try to second-guess. Improper layout can also cause dynamic errors. To avoid them, the

current-output bus of current switches (whether discrete or integrated) must be as short as possible and carefully laid out from three standpoints.

First, the longer the run from the current-summing point of the bit switches to the summing point of the output amplifier, the more likely it is to pick up extraneous EMI signals. Second, the longer the track from the output current bus to the summing point, the greater is its distributed capacitance. Third, the longer that track, the higher the inductance. This can lead to high-frequency oscillations, as mentioned previously. (NPN common-base current-sources, with  $f_t$ 's of 500MHz, can easily oscillate in the 200–300MHz region.)

Because converters interface high-speed, high-energy digital signals with high-resolution analog signals, great care is needed to minimize stray coupling of digital waveforms into the analog circuitry. For example, some D/A converters contain buffer registers to store the digital input words. All digital information is transferred with fast-rising edges of voltage and fast-changing currents. These produce radiation, which must be kept away from critical points in the analog section. A primary design rule is that the digital and analog sections be separated physically with (if at all possible) some sort of ground plate between them.

In addition, the 5V supplies used for TTL logic should be kept apart from the  $\pm 15$ V supplies normally used for analog signal processing. In particular, the ground lines from the converter to the two supplies should be kept separate and terminated only at the the power supplies themselves. This will tend to keep the fast-rising current edges in the logic sections away from the relatively stationary currents encountered in the analog sections. It is generally true that the critical points in the analog sections of the converter are of relatively high impedance. Hence they are very prone to electrostatic pickup. Even though the foregoing discussion would appear to be applicable where speed is important, high-speed transients can sometimes cause dc shifts through rectification, ringing in marginally-stable circuits, and will often require filtering of the analog output.



The faster the desired analog response, the more critical such things as digital feedthrough become, because the analog output is not ready for use until the digital transients have died away. Even though the basic electrical design goal for settling time is several hundred nanoseconds, transients coupled to the output by poor layout may result in  $1\mu\text{s}$  or greater settling time.

In the design of high-speed D/A converters for CRT display applications, digital transients due to stray coupling must be kept to very low levels. Also, the “glitches” due to intermediate states in code switching must be minimized. In Figure 14 is shown a DAC-10DF, a high-speed D/A converter specifically designed for CRT applications. It includes a sample-hold network to hold the output during switching, while the glitch-causing intermediate codes occur. Of greater relevance to this section, is the attention paid to layout considerations.

The digital section is separated from the analog sections as though a physical barrier existed on the board of the MDA-10F D/I converter module. All the input lines enter through an edge connector on the digital side of the printed-circuit card. All those lines that pass into the analog section are prefiltered by a ferrite-bead, ceramic filter-capacitor combination. For complete isolation, the analog output is not brought back to the edge connector, since it would have to pass through the digital section once again. Instead, a 90-ohm-cable connector is provided at the analog end of the board. The additional module shown in the photograph is the “deglitcher” circuit that minimizes transients resulting from the

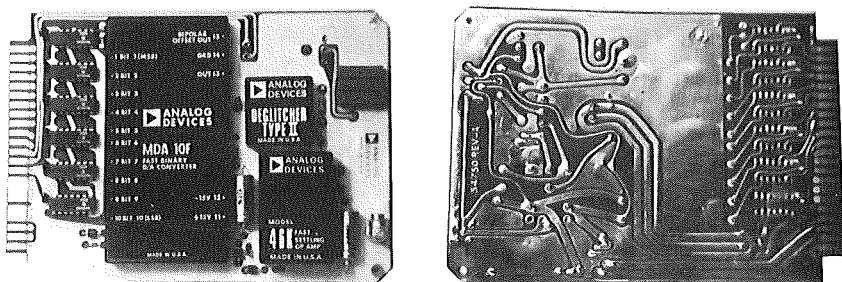


Figure 14. Deglitched High-Speed Display D/A Converter

unavoidable glitches that occur at the switch outputs during code changes.

## SUCCESSIVE-APPROXIMATION A/D CONVERTERS

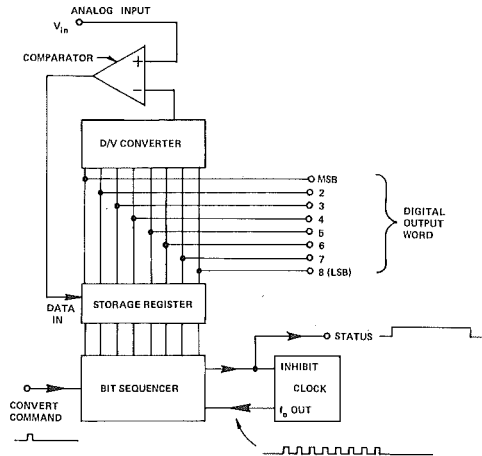
Of all the techniques for analog-to-digital conversion in use today in data acquisition systems, "successive approximations" is perhaps the most widely used. A simplified block diagram of a converter using this technique is shown in Figure 15. The basic idea of successive approximation is simple, as explained in the preceding chapter. In somewhat more detail:

When the appropriate logic signal is applied to the *convert command* input terminal, the D/A switches are set simultaneously to their "off" state, except for the most significant bit (MSB), which is set to logic "1". This turns on the corresponding D/A switch,\* which applies the analog equivalent of the MSB to the comparator. Simultaneously an internal clock is released from the *inhibit* state and allowed to free-run. Until the first clock-pulse edge arrives, the MSB is being compared with the analog voltage. (The scheme shown is only one of several ways). When the first clock pulse arrives, the MSB has shown itself to be either too "heavy" or too "light."

If the analog input voltage is less than the MSB weight, the MSB will be switched off at the first leading edge of the clock pulse; if the analog input is greater than the MSB, the "1" will remain in the register. Besides enabling the MSB decision, the clock pulse simultaneously turns on the second bit. During the period of the second pulse, the sum of the result of the first choice and the second bit is being compared with the analog input voltage. The comparator's state, when gated by the next clock pulse, will cause the register to either accept or reject that bit. In a similar manner, succeeding clock pulses cause the bits, in order of decreasing significance, to be tried, and accepted or rejected, until the LSB is finally accepted or rejected.

During this conversion time, the output of a *status* flip-flop is in its "busy/not valid" state, indicating that a conversion is taking place;

\*If complementary logic is necessary, as is typical of D/A converters using the AD550  $\mu$ DAC elements, this would be "0," as discussed in "Complementary Codes" in the preceding chapter.



**Figure 15. Block Diagram of Successive-Approximations A/D Converter**  
it signals the end of a conversion by returning to its “ready/conversion valid” state.

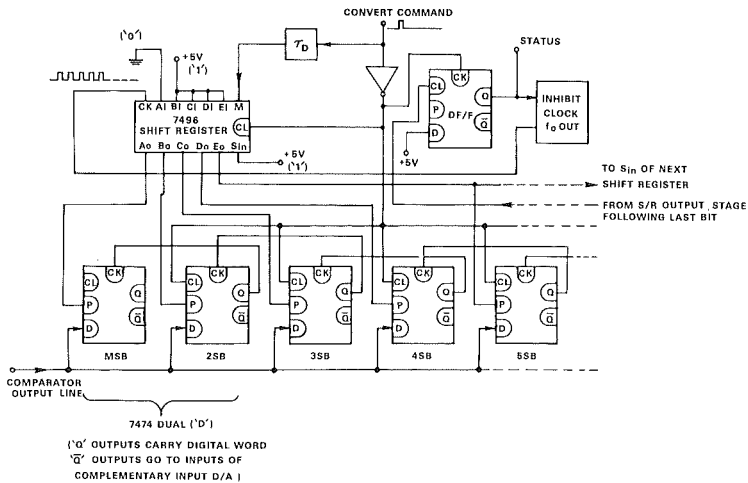
Data from the parallel output lines of a successive-approximation converter are not valid until the end of conversion. However, in some applications, it is desirable to read out the data serially. When this is done, as it is in many successive-approximation converters, one must be careful to accept the serial data only as each bit becomes valid (such as on the leading edge of each clock pulse). Hence, after each bit decision is made, the data becomes valid, and the bit can be immediately shipped serially down a data line. Serial data can also be obtained at any later time if the parallel data is “jammed” into a shift register which can then be interrogated at will. Serial data should not be taken from the comparator output, unless it is bistable, since ambiguous levels (comparator in the linear range) can cause erroneous serial output if the internal/flip-flop and external shift register have different thresholds. Ignoring this consideration will result in errors as large as  $\frac{1}{2}F.S.$

## THE LOGIC SEQUENCER

Since modern integrated-circuit logic families are continually in a state of change, it is difficult to say that any one particular logic scheme is “best.” A number of criteria determine suitability of a logic scheme for a given application. For example, it may be necessary to minimize the number of logic elements used; or to minimize

The scheme in Figure 16 can be considered representative among

### CONVERT COMMAND



**Figure 16. Logic Diagram of Successive-Approximations ADC**

\*Complementary logic

preset. As previously, its Q, going to the 1 state, clocks data on the D line into the 2nd-bit flip-flop. And so the sequence goes until the LSB is reached, at which time the *status* flip-flop trips and terminates the conversion (and inhibits the internal clock).

A new logic scheme, of growing popularity, hinges on the use of 8-bit addressable latches, recently available from several logic manufacturers. Basically, this MSI element consists of 8 latch-style flip-flops. The individual flip-flops are addressed by a 3-bit input code to the MSI element. This address simply enables the D line to that particular flip-flop. To sequence this arrangement, a 3- or 4-bit counter is used. A note of caution, however: the timing between clock pulses is somewhat more critical, because the addressable latch must be disabled and enabled between address changes to avoid changing the data in intermediate states in the addressable latch.

## COMPARATORS: THE MOST CRITICAL ELEMENT

Many IC comparators are available on the market today, and the number continues to increase. Simple in concept, but tricky in practice, these intriguing circuits are a never-ending challenge to IC designers and users alike.

The ideal comparator would have infinite gain and zero comparison time. Practical comparators are limited by parameters similar to those of op amps: open-loop gain, slew rate, bandwidth, and dc and dynamic differential input characteristics. Beyond these, comparators are further distinguished by the availability of such features as *enable* terminals and output drive capability.

There are basically two different ways in which a comparator can be used: To compare voltage, differentially, and to compare current. In the voltage mode, the analog output of the D/A converter is in a voltage form (for instance, from the output of an amplifier) and is presented at the inverting input of the comparator. The analog input voltage is connected to the noninverting terminal. Comparators used in this scheme must have high common-mode input range and excellent common-mode rejection. For instance, a 12-bit converter should have at least 96dB of CMR to keep common-mode

error well below  $1/10\text{LSB}$ . The voltage mode is generally used in situations where the analog output from the D/A is restricted to the zero-to-1-volt region (e.g., by taking the output from a resistive load on a current-output D/A). The analog input is scaled down by the proper amount and applied to the  $+$  input of the comparator, while the 1-volt D/A output is applied at the minus input.

The use of comparators in the *current* mode is perhaps more common these days, because it allows better speed and temperature tracking, and places no severe requirements on the comparator's common-mode rejection. This is particularly well-implemented with the quad-current-switching D/A's discussed earlier in this chapter. Figure 17 shows why. The  $5\text{k}\Omega$  gain resistors that are normally used as the op amp feedback element to convert current to voltage in a DAC are used as the input scaling resistors. The summing point (pin 22, AD850) is connected to the minus input of the comparator. The plus input is returned to analog signal ground through an appropriate bias-current cancellation resistor (5 or  $10\text{k}\Omega \parallel 15\text{k}\Omega$ , for single-ended converters, additional  $\parallel 6\text{k}\Omega$  for bipolar converters). By doing this, we make use of the temperature tracking of the resistors of the AD850L network to retain near-perfect gain tracking.

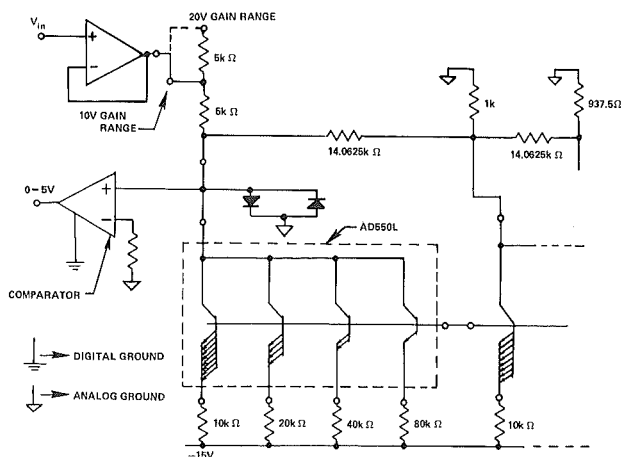


Figure 17. ADC Using Comparator in the Current Mode

The “window” determines the conversion accuracy one can obtain with any given comparator. The *window* is that range of input voltage over which the comparator output is traversing the linear region, between logic thresholds, and as such is a measure of the open-loop gain of a comparator circuit. For example, if the analog input is from 0 to +10V, and it is desired to perform a 12-bit conversion, the window must be less than 1mV for the conversion to be within one-half LSB (neglecting quantization uncertainty). Since the output of the comparator must swing between 0.4 and 2.4V to effect logic changes (TTL), the open-loop gain required for 12 bits is at least 2000. However, in practice, this figure should be at least 5000 to minimize the errors due to finite open-loop gain.

Besides gain, dc offset and drift, and impedance level, another spec that must be carefully considered in the selection of a comparator is its *speed*. The typical performance of integrated circuit comparators available today is specified by means of response diagrams on data sheets. A typical plot is shown on Figure 18; it can be seen that the speed is sharply influenced by the amount of overdrive of the comparator. The amount of overdrive applied to a given comparator in an A/D application depends on the input voltage range used and the resolution sought. The designer must be careful to plan for the minimal amount of overdrive appropriate to any given application.

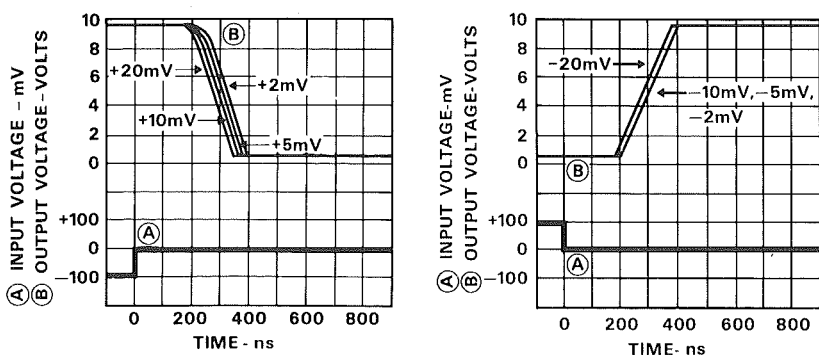


Figure 18. Comparator Response as a Function of Input Overdrive (Type AD351)

The most troublesome aspect of using any comparator, be it discrete or integrated, is the problem of maintaining frequency stability

while within the linear region (i.e., in the “window”). Although the comparator is like an operational amplifier with no overt feedback, it is operating at high gain-bandwidth, with minimal feedback compensation. Even small amounts of parasitic feedback, either directly around the device, or via the power supply leads, can cause oscillation. These oscillations are generally caused by improper layout, for example, in separating the fast-rising output edges from the high-impedance input points. It is intuitively obvious that capacitive coupling of fast edges to the negative input could develop ringing or sustained oscillation when the net input is in the “window” region.

For this reason, it is recommended that adequate shielding, e.g., by ground plane, be used between the input and output. Also, it is wise to keep the digital ground terminal (normally returned to the output transistor of a comparator) away from the analog input grounds and signal lines. Furthermore, for IC comparators (whether the data sheet suggests it or not), it is a wise idea to buffer the load driven by the comparator output with a discrete transistor. This not only leads to a higher gain in the comparator, but will also lighten the changes in power dissipation in the internal output transistor, thereby eliminating thermal feedback effects.

The effect of an oscillating comparator on the A/D conversion is: as the analog input approaches the edge of a quantization level, the codes become indecisive, and in fact, exhibit non-monotonic behavior. For example, one can raise the analog input voltage sufficiently to increase the code by 1LSB, and then find that, for a slight further increase in analog input, the code goes back to the original digital output. This often-troublesome behavior can be cured in a rather surprising way — elimination by “size.” If the comparator gain is *increased*, such that the window size is reduced to a very small fraction of the total LSB weight, then the region of each code over which the oscillation occurs is reduced to an infinitesimal amount, approaching a magnitude comparable to that of the circuit background noise.

## OTHER CONSIDERATIONS IN A/D CONVERTER DESIGN

The additional error sources that can occur when a D/A converter is used in A/D conversion are primarily centered around the



comparator's input and gain characteristics. In particular, offset drift and input bias-current drift are important in the selection of a comparator. Further errors are introduced by extraneous noise pickup in the analog sections due to fast-rising and changing edges of nearby digital logic.

Hence it is most important that much consideration and effort be given to adequate separation between digital and analog components in the circuit layout. Once again, the digital power supply should be kept entirely separate from the analog power supply, the analog input signals, and the D/A output section. This separation should be physical as well as electrical. One should take great care to minimize the *number* of digital signals that must be brought into or near the analog sections.

Another aspect that can spell trouble if not anticipated is the adequacy and use of the conversion time. Two factors place lower limits on this to a significant degree: one is the settling time of the D/A output, the other the switching time of the comparator.

Since the D/A output is driving the comparator towards its new value, the switching times of both elements are accumulated, but not in purely additive fashion. A useful trick is to use the fact that the most-significant bits take much longer to settle to their final values than do the LSB steps of a successive-approximations converter. Hence, to speed the overall conversion time one can use a frequency-modulated clock having decreasing period as the conversion progresses.

